ANDY100 EVALUATION BOARD WITH INTEGRATED START-UP CIRCUIT

Check for samples: SPIDER-H254

DESCRIPTION

SPIDER-H254 is an EPC Class-1 Generation-2 (C1G2) RFID tag based on Farsens' batteryless sensor technology. Built in a compact PCB format, the tag is intended to be used as development platform for new battery free wireless sensor or actuators.
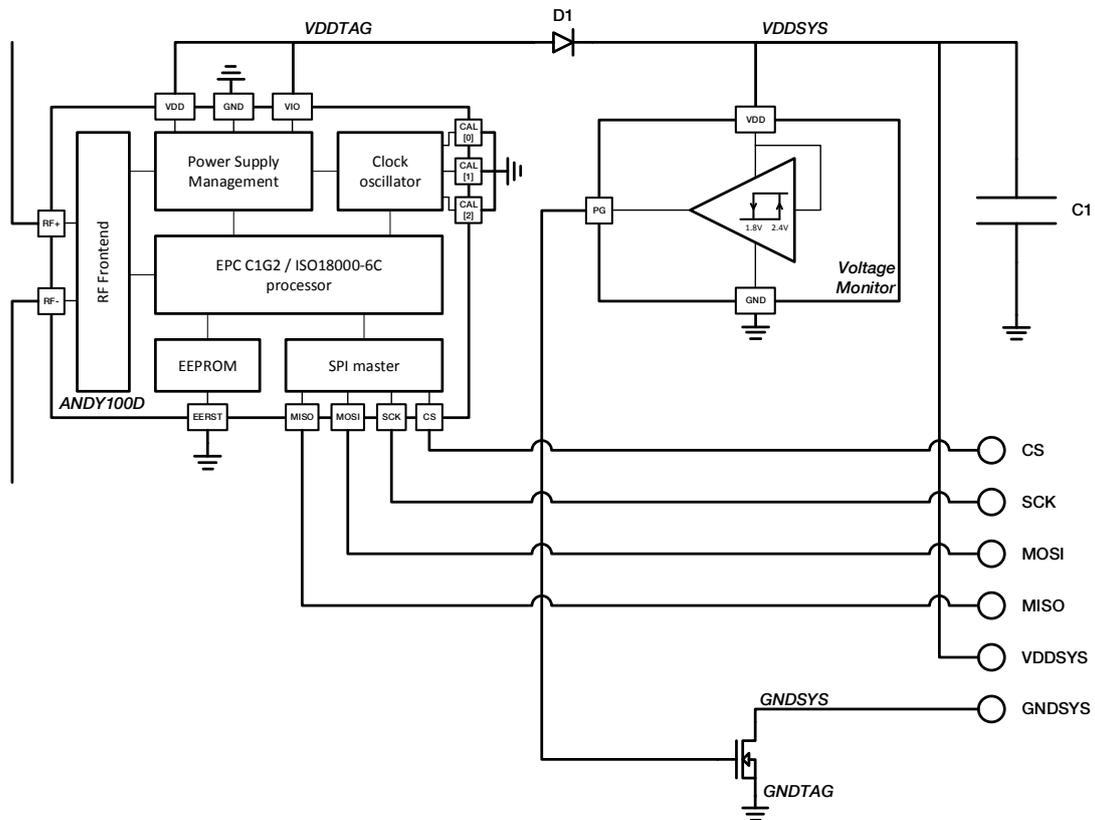
The RFID interface is compatible with commercial UHF RFID readers (EPC C1G2). With a 2W ERP setup the battery-less tag can communicate to over one meter and a half - 5 feet. The actual distance will depend on load connected to the SPIDER-H254 .

The SPIDER-H254 is available in a variety of antenna design and sizes, depending on the specific application. It can be encapsulated in an IP67 or IP68 casing for usage in harsh environments.

BLOCK DIAGRAM

The SPIDER-H254 tag consists of an ANDY100 IC for energy harvesting and wireless communication, a start-up circuitry based on a voltage monitor and a external connector.

The ANDY100 IC includes a RF frontend for UHF RFID power harvesting and communication, a power supply module to generate the required voltage levels, a EPC C1G2/ISO18000-6C digital processor including a trimmed clock oscillator, a non volatile memory and a SPI master module. The SPI master module can be controlled via EPC C1G2 standard memory access commands.

FEATURES

- **860MHz-960MHz operation**
- **EPC Class-1 Generation-2 compliant**
- **ISO 18000-6 Type C compliant**
- **96-bit EPC & 32-bit TID**
- **Embedded start-up circuit**

In order to isolate the supply of the RFID tag from the supply of the rest of the system, the diode D1 is included. The capacitor C1 acts as an energy storage unit to support current peaks of the system during active operation, such as initialization and active operation.

A voltage monitor is included to connect external loads only after the energy storage capacitor has been charged. The voltage monitor connects the external load when the voltage in the capacitor is over 2.4V and disconnects it when the voltage falls below 1.8V. This architecture avoids oscillation of the system during the startup.

The SPI communication lines of the ANDY100 and the isolated power signals are available at an external connector to evaluate the ANDY100 IC with external components.

CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
RFID					
RF_{SENS}	RF sensitivity fully passive	-4	-2	0	dBm
OPERATING CONDITIONS					
T_{OP_TOP}	Operating temperature range	-30		85	°C

SPIDER CONNECTOR

The SPIDER board has a external connector to facilitate access to the most important signals of the system.
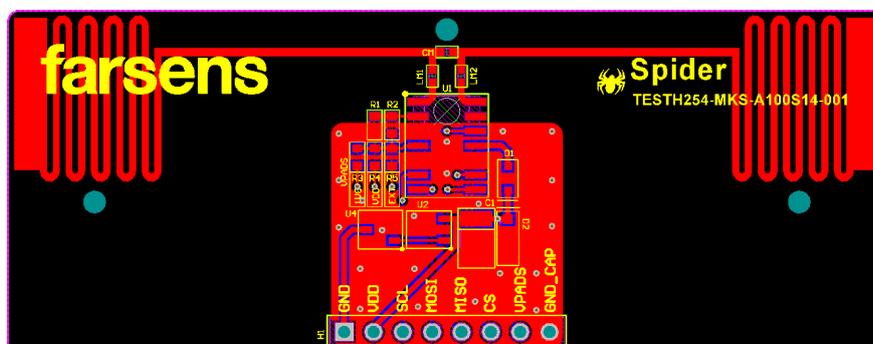
H1: POWER & SPI

PIN	Description
GND	Isolated ground
VDD	Isolated supply
SCL	ANDY100 SCL
MOSI	ANDY100 MOSI
MISO	ANDY100 MISO
CS	ANDY100 CS
VPADS	IO pads supply
GND_CAP	Non isolated ground

External systems can be connected to VDD-GND, so that they will be only activated once the tag has harvested and stored enough energy on the supply capacitor. The start-up circuit is configured to connect the external load once the supply capacitor exceeds 2.4V.

The SPI signaling works through the pins SCL, MOSI, MISO and CS. The tag is the master device, so any external device shall be configured as slave.

The VPADS pin can be used either to pass the pad supply from the tag to the external system or to pass an external supply to the internal pads. The next section describes how to configure the IO supply.

Finally, GND_CAP is accesible in case the supply capacitor has to be increased. An additional capacitor can be connected between VDD and GND_CAP in order to do that.

VDDPADS: IO SUPPLY

In order to make the system work, it is necessary to configure the internal VDDPADS pin of the ANDY100 to have a stable voltage. **Do not** power up the device with VDDPADS floating, or the ANDY100 may be damaged.

In order to use different configurations, the VDDPADS pin of the ANDY100 can be connected to different nets by means of the resistors R3, R4 and R5. The following table shows the different possible configurations.

Option	R3	R4	R5	Description
1V8	0Ω	NC	NC	VDDPADS connected to internal 1V8 LDO of ANDY100. External VPADS pin floating.
	0Ω	NC	0Ω	VDDPADS connected to internal 1V8 LDO of ANDY100. External VPADS pin can be used to supply IO of external devices.
VDD	NC	0Ω	NC	VDDPADS connected to isolated VDD. External VPADS pin floating.
	NC	0Ω	0Ω	VDDPADS connected to isolated VDD. External VPADS pin can be used to supply IO of external devices.
EXT	NC	NC	0Ω	VDDPADS connected to external VPADS. External VPADS pin **must** be supplied externally. Failing to do so may damage the ANDY100 device.

OPERATION

EPC reading

In order to read the EPC of the tag, commercial EPC C1G2 readers can be used. However, some considerations have to be taken into account.

As the tag has a significant supply capacitor connected to VDD, the power-up of the system will be slow. It can last several seconds. In order to speed up the charge process, the reader shall be configured to send power as continuously as possible. Refer to the application note *External capacitor on VDD of ANDY100* for detailed instructions on how to set up the reader for best performance.

Once the supply capacitor is charged, the tag will respond with its EPC. From this point on, memory access commands can be used to control additional functionalities via the SPI bridge.

SPI bridge

ANDY100 includes specific hardware for master SPI operation. This hardware uses the SPI configuration CPOL=1 and CPHA=1, which is commonly known as mode 3. The serial interface interacts with SPI slaves with 4 wires: CS, SCK, MOSI and MISO.

CS is the Chip Select signal which enables the slave device. The master drives this signal low at the start of the communication and drives it back high at the end.

SCK is the serial clock and it is driven by the SPI master. In mode 3 the idle state of the SCK line is high.

MOSI and MISO are respectively the Master Output Slave Input data port and the Master Input Slave Output data port. These lines are driven at the falling edge of SCK and should be captured at the rising edge of SCK. MOSI is driven by the master whereas MISO is driven by the slave. After a succesful communication, the master drives the MOSI signal high into the idle state.

The SPI master includes fixed read register and write register commands. Both of them are completed in 16 clock pulses or in multiple of 8 in case of multiple bytes read. Bit duration is the time between two falling edges of SCK. The first bit (bit 0) starts at the first falling edge of SCK after the falling edge of CS while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SCK just before the rising edge of CS.

Command structure

ANDY100 can perform read register and write register operations. Both of them can be used to perform a single register access or multiple register access. The command structure in the SPI interface is shwon in figure **??**.
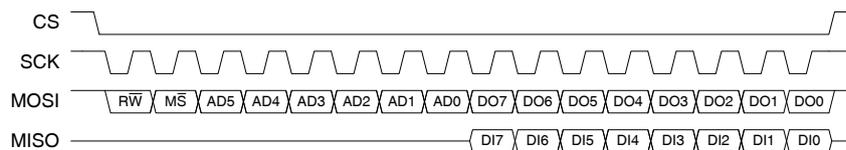

Figure 1: SPI command timing diagram.

bit 0:   RW bit. When 0, the data DO(7:0) is written into the slave device. When 1, the data DI(7:0) from the slave device is read.

bit 1:   MS bit. When a multiple read operation is requested, this bit is set to 1. The slave device should increment the register address automatically every 8 cycles of SCK.

bit 2-7:   address AD(5:0). This is the address field of the indexed register.

bit 8-15:   data DO(7:0) (write mode). This is the data that is written into the device (MSb first).

bit 8-15:   data DI(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read commands further blocks of 8 clock periods will be added.

When a read or write operation is commanded from the EPC C1G2 interface pointing to a memory address mapped to the SPI bridge, the corresponding signaling is generated in the SPI interface. If a single word read is requested from the EPC C1G2 side, a single register read will be executed. If several words are requested within the same EPC C1G2 read command, a multiple register read will be executed. If a word write is requested from the EPC C1G2 interface, a single register write will be executed in the SPI interface.

The address used in the adress bits of the SPI signaling is the address of the register inside the User bank of the EPC C1G2 memory space. The values of RW and MS are set depending on the requested operation.

Read command

Figure **??** shows the timing diagram of the SPI signaling executed upon the reception of a EPC C1G2 read command containing a single word mapped to the SPI bridge.
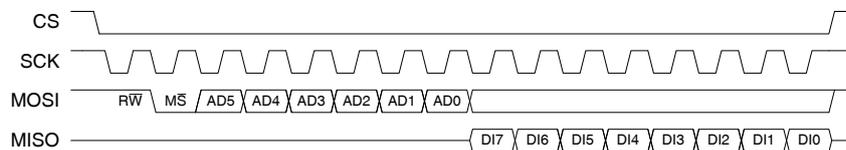

Figure 2: SPI single read timing diagram.

Figure **??** shows the timing diagram of the SPI signaling executed upon the reception of an EPC C1G2 read command containing two words mapped to the SPI bridge. If more words are requested in the read command, the SPI master will issue more SCK cycles until all the SPI registers have been read.

The SPI master included in ANDY100 can execute multiple register read commands of up to 6 registers. If more than 6 registers have to be read, this has to be done issuing separate read commands.
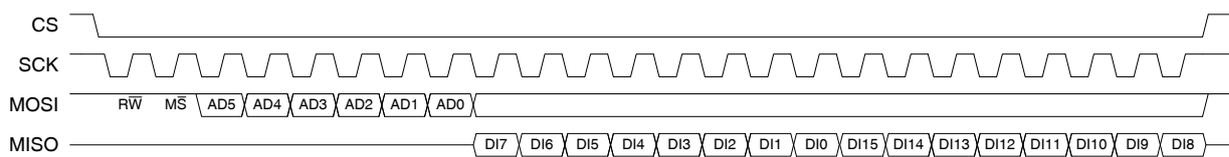

Figure 3: SPI multiple read timing diagram.

In the response to EPC C1G2 read commands, ANDY100 includes the data that has been read in the MISO line during the SPI communication. The register word length used in the SPI interface is 8 bits whereas the length of the EPC words is 16 bits. The data of the SPI register word is right aligned inside the word of the EPC register in the answer to the reader. Thus, all the data read from the SPI bridge will contain 8 initial 0's followed by the value of the SPI register in each word.

Write command

Figure **??** shows the timing diagram of the SPI signaling executed upon the reception of a EPC C1G2 write command addressed to a word mapped to the SPI bridge.
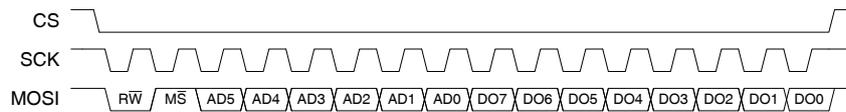

Figure 4: SPI write timing diagram.

As for the read command, the word length conversion between EPC C1G2 and SPI memory spaces is done by right aligning the 8 bit SPI word inside the 16 bit EPC C1G2 word.

DEMO SOFTWARE

Demonstration software to read and control the SPIDER-H254 is available in the web. Download the latest software and user guide at: http://www.farsens.com/software.php. Currently, the software is compatible with the following UHF RFID readers:

Fixed readers

- Alien ALR9900

- AMS Radon

- Caen Muon DevKit - RS232

- CSL CS203

- Impinj R420

- Thingmagic M6

- Thingmagic M6e DevKit6

- Motorola FX9500

- Motorola FX7400/FX7500

- Nordic ID Sampo

- Nordic ID Stix

- RF-Embedded PUR500U

- Sirit IN610

Handheld readers

- Nordic ID Merlin

- Nordic ID Morphic

- Motorola MC9090G

- Motorola MC9190Z

REFERENCES

The next table shows the available references of the SPIDER-H254.

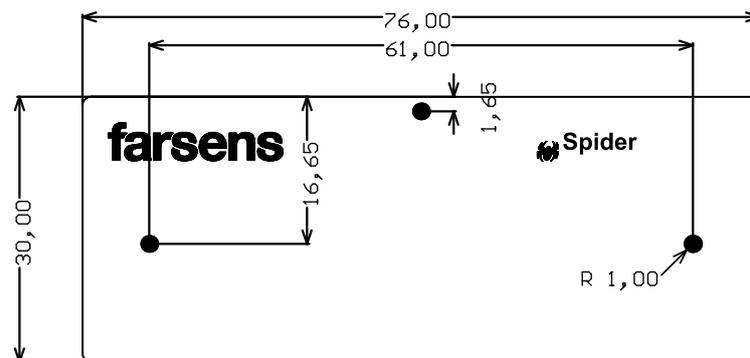| Ref.	Name	Description
34802	SPIDER-H254-MKS	SPIDER-H254, meander wideband antenna, PCB format

For custom references with other antennas and housings, please contact us at info@farsens.com.

MECHANICAL DIMENSIONS

All dimensions are in millimeters.

MKS

Valid for reference(s): 34802

Maximum height: 3mm